

Project Notes

This schematic generally follows what was published in Radio Magazine No.5, 1986 with the following exceptions:

- 16k DRAM (D22..D29) is replaced with 32k SRAM in a single IC (D22)
- D16, D17, D19, R20..R28 and the associated circuitry around DRAM are removed
- The circuit limiting the length of RESET pulse (C1, R2) to prevent DRAM decay is eliminated; an on-board reset button is added
- \overline{WR} buffer (D5.4) is removed
- EPROM is replaced with EEPROM: 2816 (D17) with AT28C64 and 2808 (D12) with AT28C16
- Bigger font ROM allows two fonts to be programmed; font selection is implemented via GPA0 video attribute (see i8275 documentation)
- \overline{CS} decoder is changed to provide additional \overline{CS} signals for 4k memory blocks starting at 9000h, B000h, and D000h
- Additional decoupling capacitors are provided (C101-C114)
- Speaker (H1) is replaced with on-board piezo transducer; C26 is eliminated
- A separate pixel clock (PIXEL_CLK) is used for video clocking instead of CPU clock
- A single 61-pin connector is replaced with two 26-pin boxed headers (one per i8255), three pairs of wire pads (composite video, tape in and tape out), DC power pads, and a RESET header

Project Notes

TITLE: Radio-86RK-SRAM_R2

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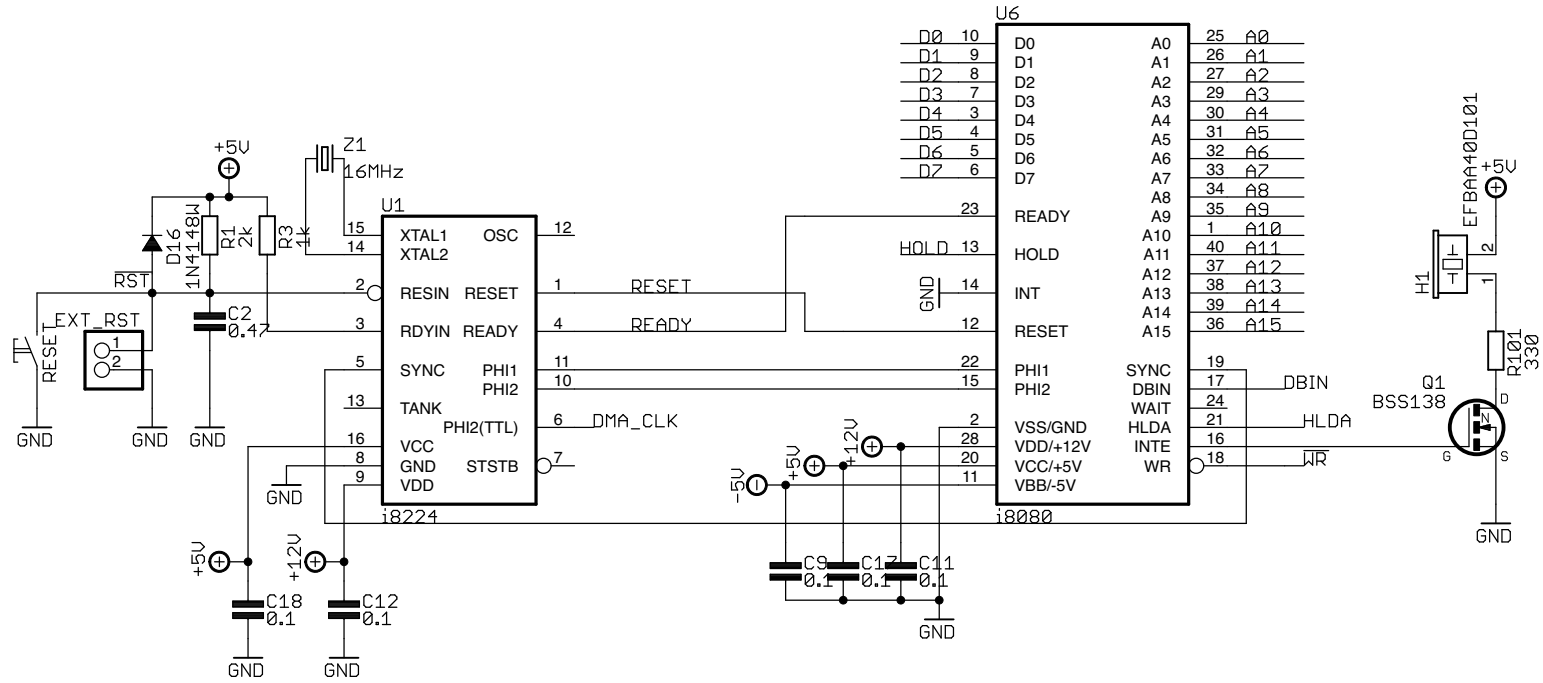
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Clock and reset

CPU



CPU and Clock

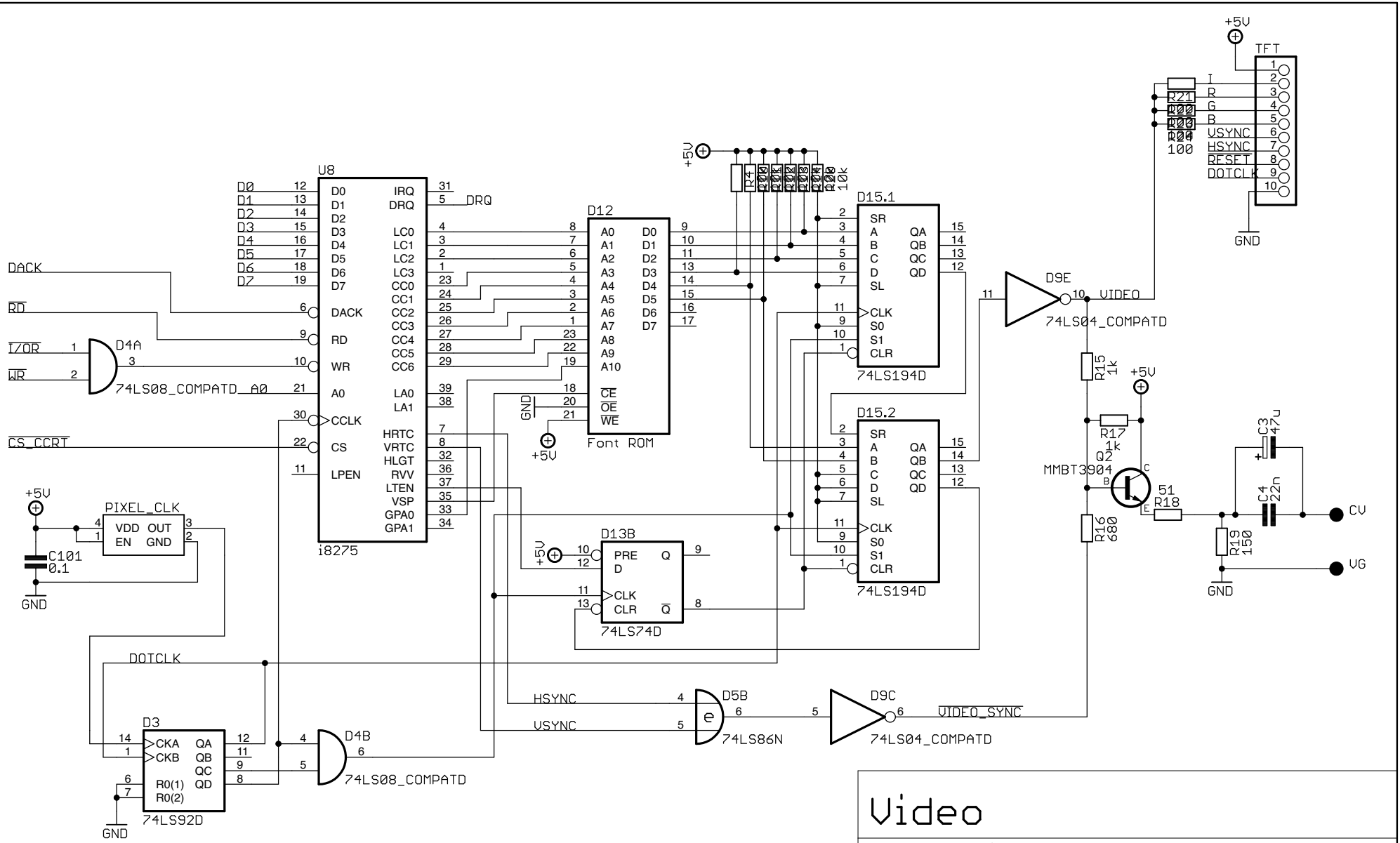
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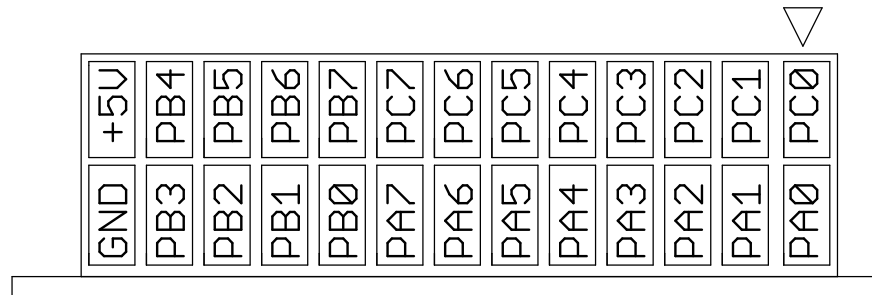
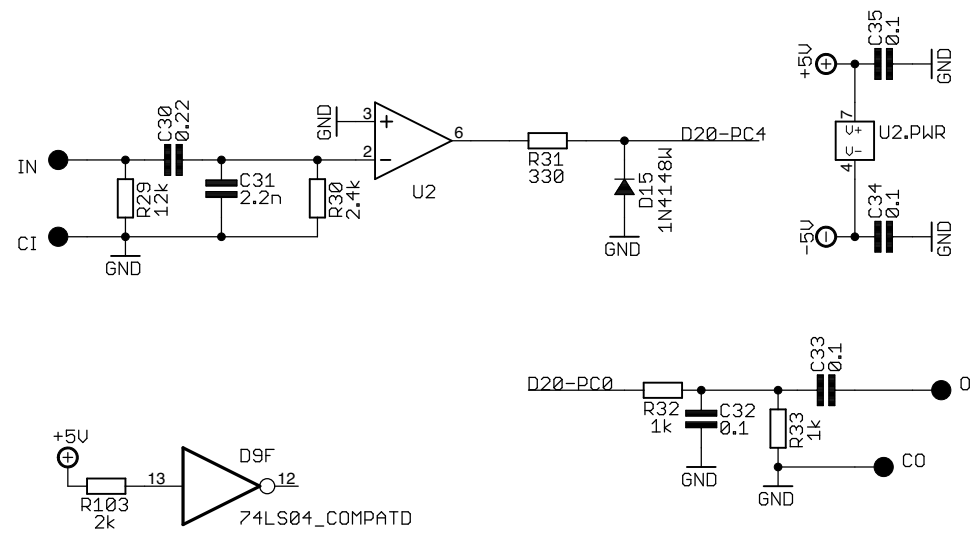
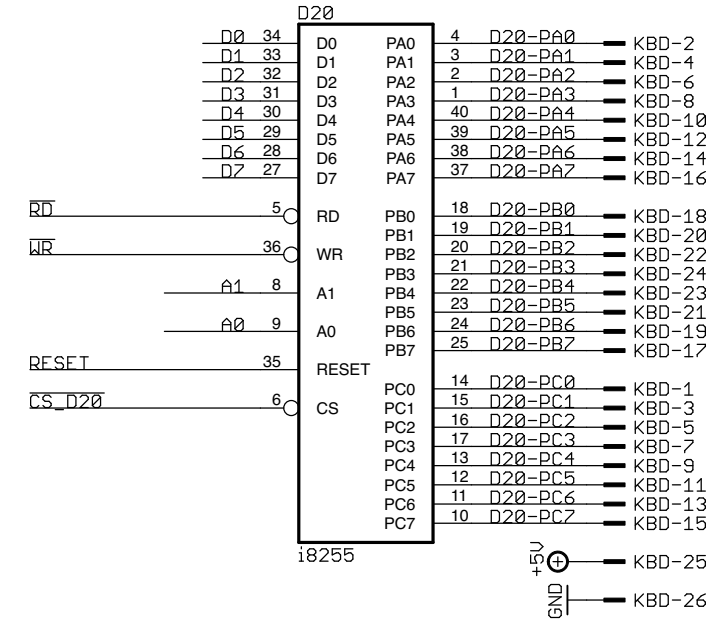
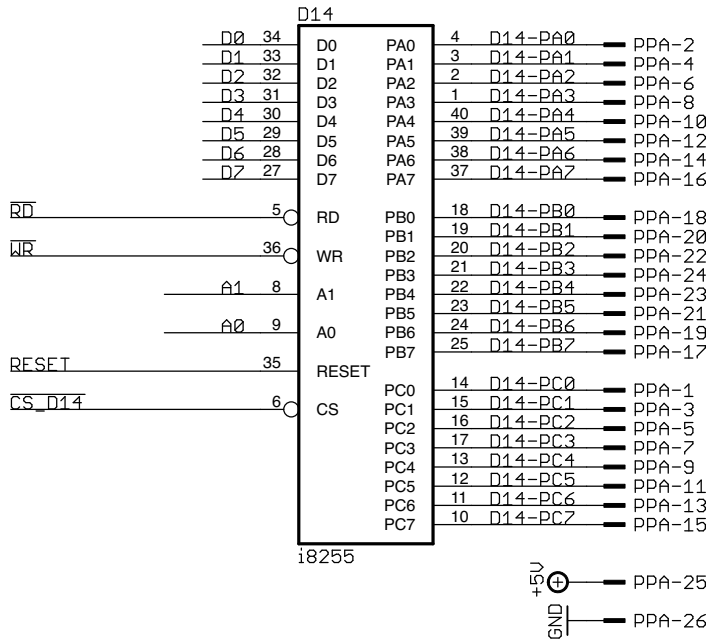
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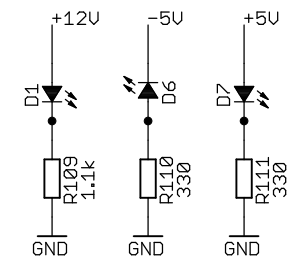
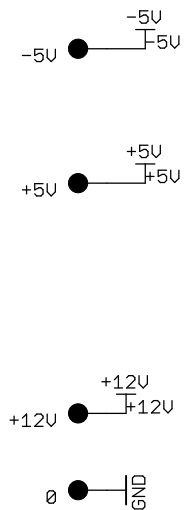
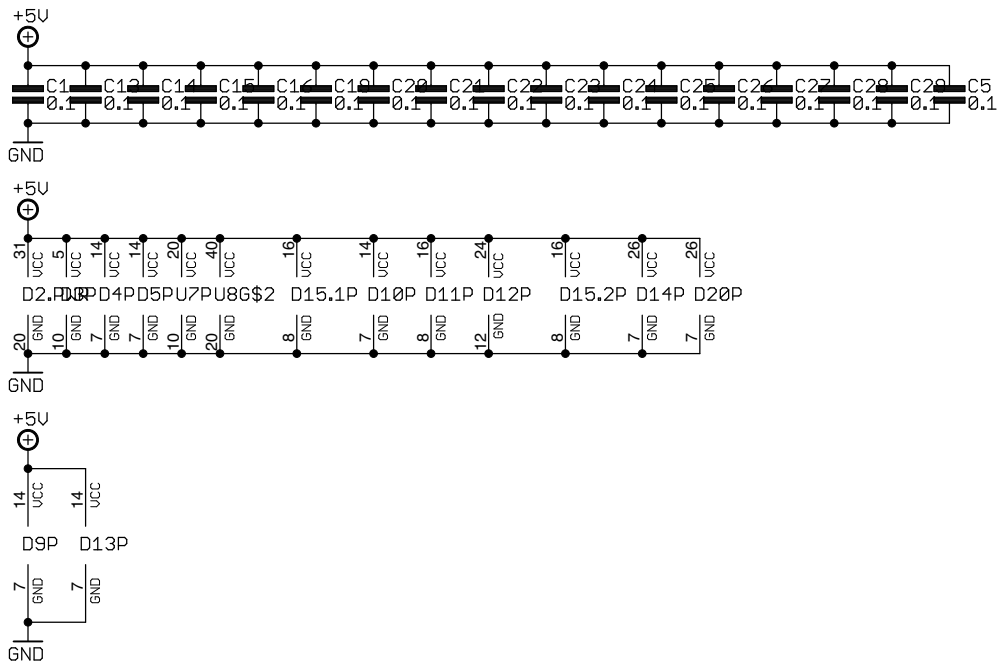
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<h1>Video</h1>	
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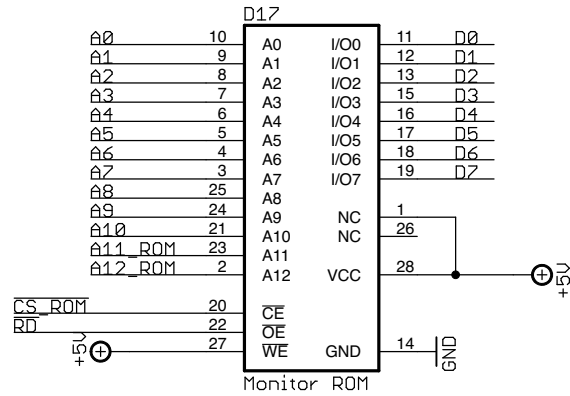


<h1>I/O</h1>	
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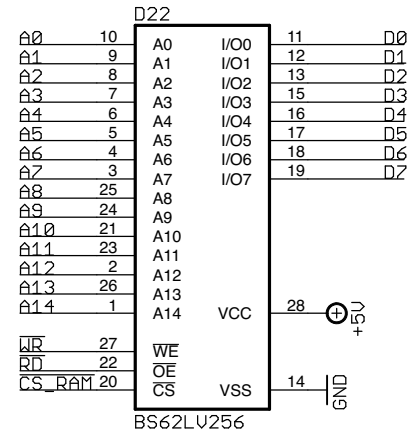


<h1>Power Supply</h1>	
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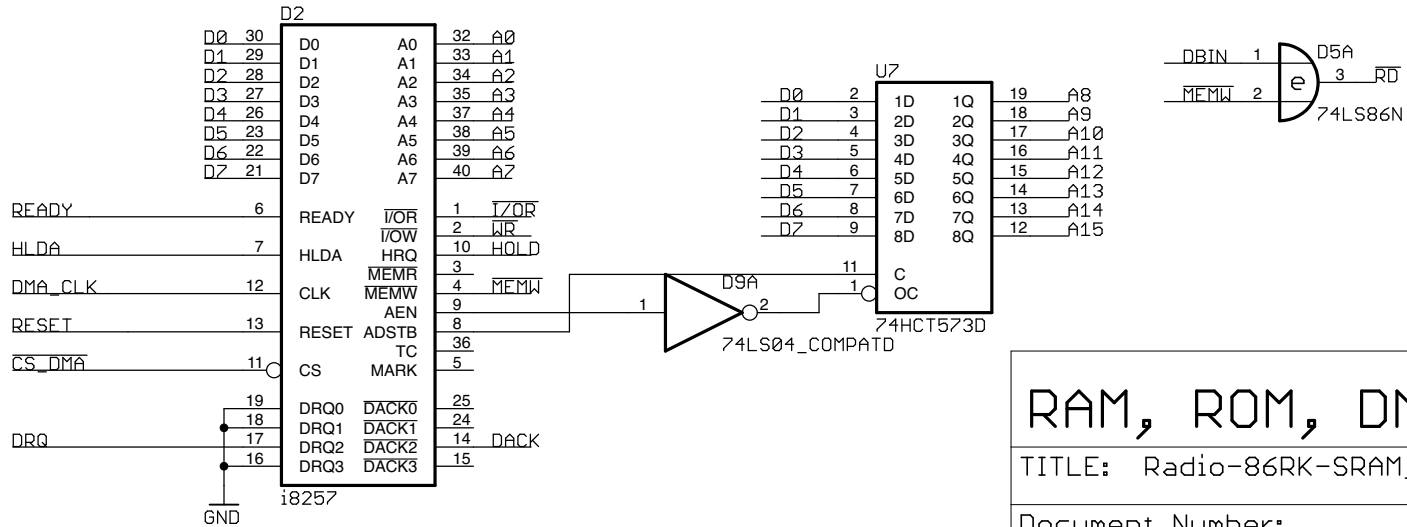
ROM



RAM

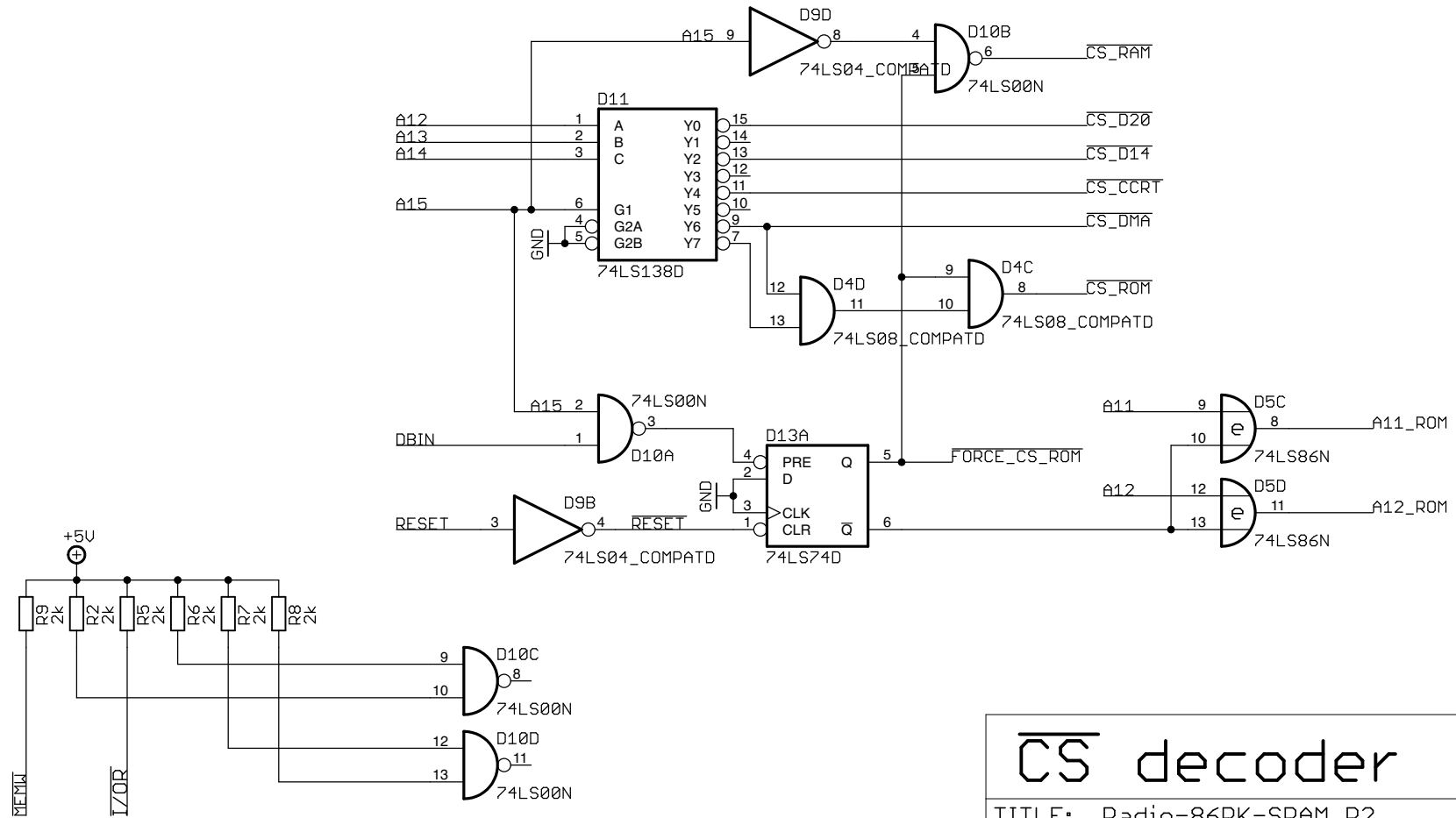


DMA



<h2>RAM, ROM, DMA</h2>	
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\overline{CS} decoder



\overline{CS} decoder

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