# I8255A
# PROGRAMMABLE PERIPHERAL INTERFACE

*INDUSTRIAL*

- **Industrial Temperature Range: −40°C to +85°C**
- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Improved Timing Characteristics**
- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40-Pin Dual In-Line Package**
- **Reduces System Package Count**
- **Improved DC Driving Capability**

The Intel® I8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

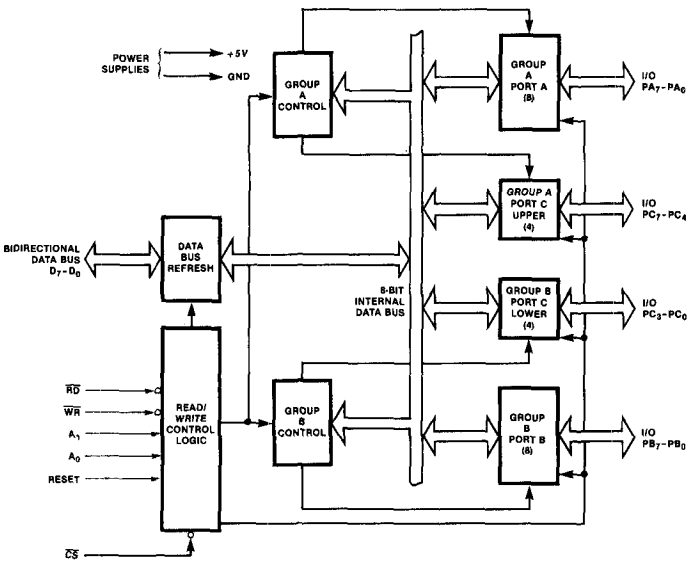
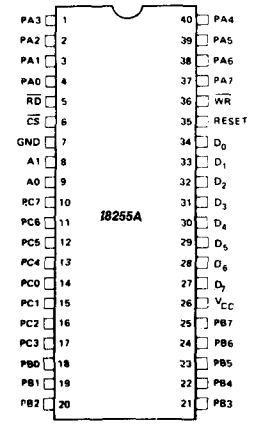



**Figure 1. Block Diagram**




| | |
|---|---|
| $D_7$–$D_0$ | DATA BUS (BI-DIRECTIONAL) |
| RESET | RESET INPUT |
| $\overline{CS}$ | CHIP SELECT |
| $\overline{RD}$ | READ INPUT |
| $\overline{WR}$ | WRITE INPUT |
| A0, A1 | PORT ADDRESS |
| PA7-PA0 | PORT A (BIT) |
| PB7-PB0 | PORT B (BIT) |
| PC7-PC0 | PORT C (BIT) |
| $V_{CC}$ | +5 VOLTS |
| GND | 0 VOLTS |

**Figure 2. Pin Configuration**

## ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## D.C. CHARACTERISTICS ($T_A$ = −40°C to +85°C, $V_{CC}$ = +5V ±5%, GND = 0V)

| Symbol | Parameter | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.2 | $V_{CC}$ | V | |
| $V_{OL}$ (DB) | Output Low Voltage (Data Bus) | | 0.45 | V | $I_{OL}$ = 2.5mA |
| $V_{OL}$(PER) | Output Low Voltage (Peripheral Port) | | 0.45 | V | $I_{OL}$ = 1.7mA |
| $V_{OH}$(DB) | Output High Voltage (Data Bus) | 2.4 | | V | $I_{OH}$ = -400μA |
| $V_{OH}$(PER) | Output High Voltage (Peripheral Port) | 2.4 | | V | $I_{OH}$ = -200μA |
| $I_{DAR}$[1] | Darlington Drive Current | -1.0 | -4.0 | mA | $R_{EXT}$ = 750Ω; $V_{EXT}$ = 1.5V |
| $I_{CC}$ | Power Supply Current | | 120 | mA | |
| $I_{IL}$ | Input Load Current | | ±10 | μA | $V_{IN}$ = $V_{CC}$ to 0V |
| $I_{OFL}$ | Output Float Leakage | | ±10 | μA | $V_{OUT}$ = $V_{CC}$ to 0V |

**NOTE:**
1. The I8255A will operate as an 8255A-5 from 0°C to 70°C.

## CAPACITANCE ($T_A$ = 25°C, $V_{CC}$ = GND = 0V)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 10 | pF | fc = 1MHz |
| $C_{I/O}$ | I/O Capacitance | | | 20 | pF | Unmeasured pins returned to GND |

## A.C. CHARACTERISTICS ($T_A$ = −40°C to +85°C, $V_{CC}$ = +5V ±5%, GND = 0V)

### Bus Parameters

**READ** [2]

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{AR}$ | Address Stable Before READ | 0 | | ns |
| $t_{RA}$ | Address Stable After READ | 0 | | ns |
| $t_{RR}$ | READ Pulse Width | 300 | | ns |
| $t_{RD}$ | Data Valid From READ[2] | | 250 | ns |
| $t_{DF}$ | Data Float After READ | 10 | 150 | ns |
| $t_{RV}$ | Time Between READs and/or WRITEs | 850 | | ns |

## A.C. CHARACTERISTICS (Continued)

**WRITE**

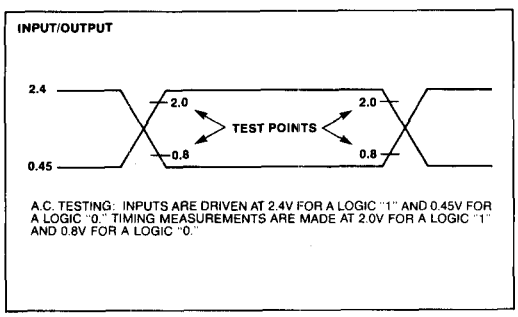
| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{AW}$ | Address Stable Before WRITE | 0 | | ns |
| $t_{WA}$ | Address Stable After WRITE | 20 | | ns |
| $t_{WW}$ | WRITE Pulse Width | 400 | | ns |
| $t_{DW}$ | Data Valid to WRITE (T.E.) | 100 | | ns |
| $t_{WD}$ | Data Valid After WRITE | 30 | | ns |

**OTHER TIMINGS** [3]

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{WB}$ | WR = 1 to Output [2] | | 350 | ns |
| $t_{IR}$ | Peripheral Data Before RD | 0 | | ns |
| $t_{HR}$ | Peripheral Data After RD | 0 | | ns |
| $t_{AK}$ | ACK Pulse Width | 300 | | ns |
| $t_{ST}$ | STB Pulse Width | 500 | | ns |
| $t_{PS}$ | Per. Data Before T.E. of STB | 0 | | ns |
| $t_{PH}$ | Per. Data After T.E. of STB | 180 | | ns |
| $t_{AD}$ | ACK = 0 to Output [2] | | 300 | ns |
| $t_{KD}$ | ACK = 1 to Output Float | 20 | 250 | ns |
| $t_{WOB}$ | WR = 1 to OBF = 0 [2] | | 650 | ns |
| $t_{ACB}$ | ACK = 0 to OBJ = 1 [2] | | 350 | ns |
| $t_{SIB}$ | STB = 0 to IBF = 1 [2] | | 300 | ns |
| $t_{RIB}$ | RD = 1 to IBF = 0 [2] | | 300 | ns |
| $t_{RIT}$ | RD = 0 to INTR = 0 [2] | | 400 | ns |
| $t_{SIT}$ | STB = 1 to INTR = 1 [2] | | 300 | ns |
| $t_{AIT}$ | ACK = 1 to INTR = 1 [2] | | 350 | ns |
| $t_{WIT}$ | WR = 0 to INTR = 0 [2] | | 850 | ns |

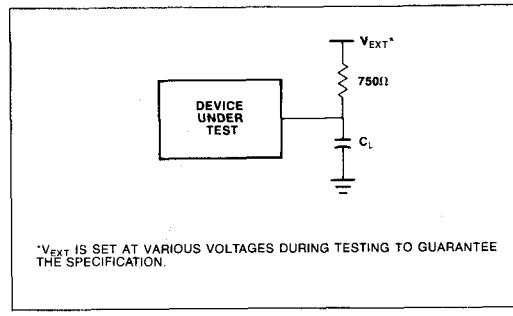
**NOTES:**
1. Available on any 8 pins from Port B and C.
2. Test Conditions: 8255A: $C_L$ = 100pF; 8255A-5: $C_L$ = 150pF.
   Period of Reset pulse must be at least 50$\mu$s during or after power on. Subsequent Reset pulse can be 500 ns min.
3. $C_L$ = 100 pF.

### A.C. TESTING INPUT, OUTPUT WAVEFORM




A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

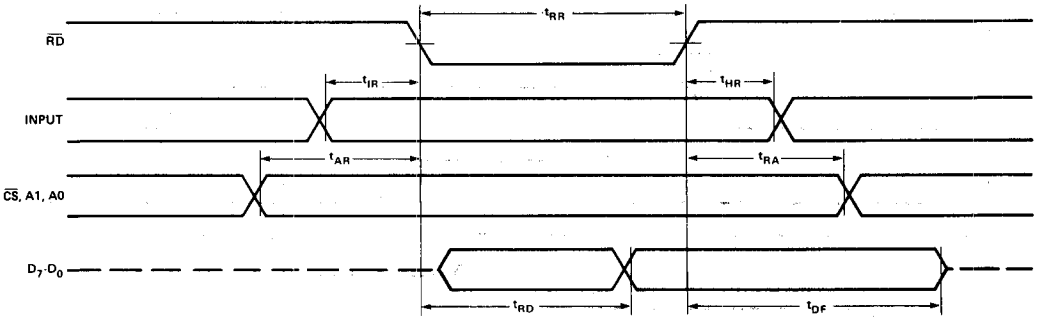
### A.C. TESTING LOAD CIRCUIT



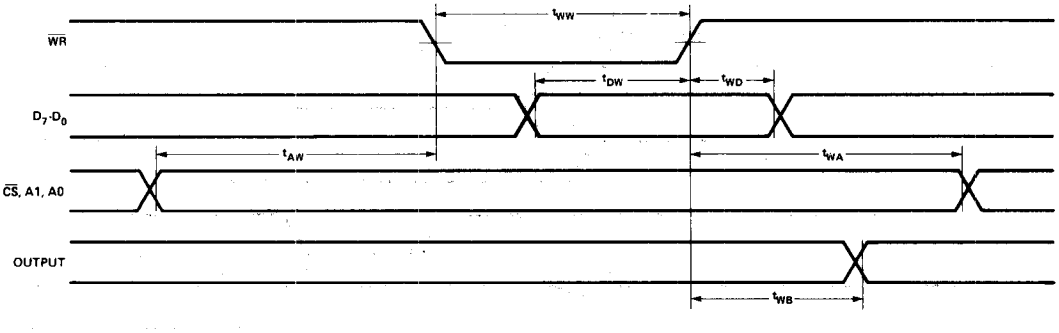

*$V_{EXT}$ IS SET AT VARIOUS VOLTAGES DURING TESTING TO GUARANTEE THE SPECIFICATION.

## WAVEFORMS

### MODE 0 (BASIC INPUT)

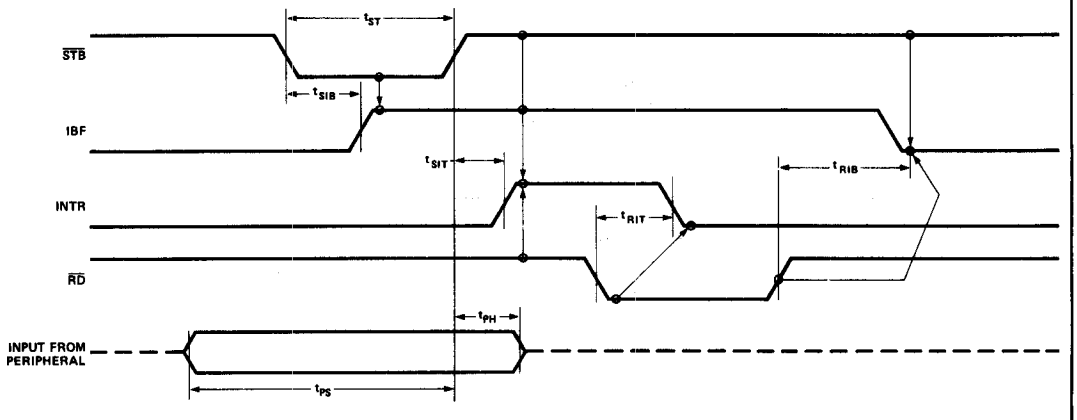



### MODE 0 (BASIC OUTPUT)

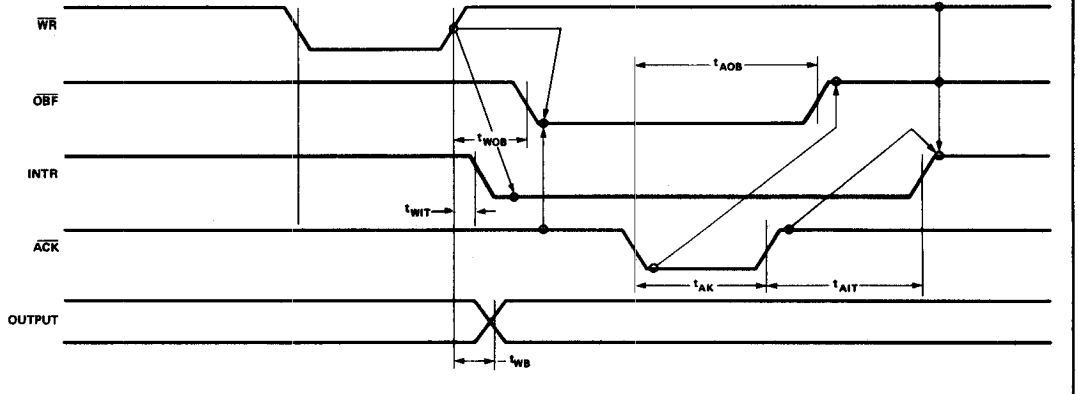


## WAVEFORMS (Continued)

### MODE 1 (STROBED INPUT)

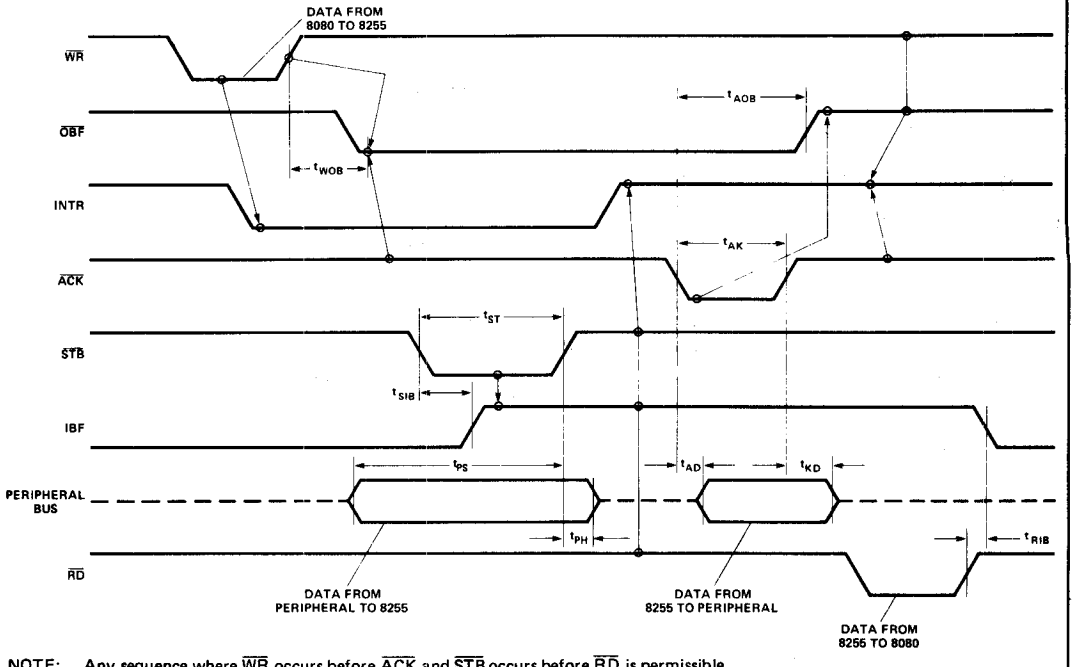



### MODE 1 (STROBED OUTPUT)



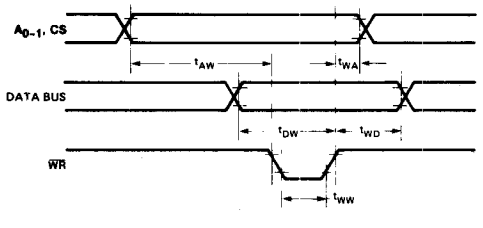
## WAVEFORMS (Continued)

### MODE 2 (BIDIRECTIONAL)




NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

### WRITE




### READ